IN THE ABSTRACT:

Please amend the Abstract as indicated below:

A method and apparatus for the implementation of reduced state sequence estimation is disclosed~~. , with an increased throughput using~~ that uses precomputation (look-ahead) to increase throughput, with only a linear increase in hardware complexity with respect to the look-ahead depth. The present invention limits the increase in hardware complexity by taking advantage of past decisions (or survivor symbols). The critical path of a conventional RSSE implementation is broken up into at least two smaller critical paths using pipeline registers. Various reduced state sequence estimation implementations are disclosed that employ one-step or multiple-step look-ahead techniques to process a signal received from a dispersive channel having a channel memory.